REMARKS/ARGUMENTS

Reconsideration of the above identified patent application is hereby requested. Claims 1 to 67 are now in the application. No claims have been cancelled or added. Claims 14 and 16 have been amended to place them in better form for U.S. practice.

The Examiner indicates that, among others, Claims 4, 5, 8, 9, 20 , 22, 24, 25, 38, 39, 43, 49, 50 and 56 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Accordingly, the Applicants have amended Claims 4, 5, 20 , 22, 38, 39, 43, 49, 50 and 56 to include the limitations of the base claim and any intervening claim, and as such these claims are now believed allowable. Claims 8 and 9 are dependent on Claim 5. As such, Claims 8 and 9 are believed allowable based upon Claim 5 and for the additional limitations contained therein. Claims 24, 25 and 26 are dependent on Claim 22. As such, Claims 24 and 25 are believed allowable based upon Claim 22 and for the additional limitations contained therein.

The Examiner alleges that the filing date for the Application will be given the date of the parent application 09/548,400, which is 4/13/00. Specifically, the Examiner alleges that the provisional application 60/136,685, filed on 5/28/99, fails to disclose anything related to the claims.

However, Claim 1 of the present Application calls for, "A method of synchronizing data clocked by a first clock to a second clock, comprising deriving an offset between the first clock and the second clock, and fractionally resampling the data as a function of the offset." In comparison, Paragraph 4 of the

provisional application 60/136,685 discloses that, "The objective of the sampling rate tracker is to generate outputs in such a way so that the distance between the write and the read pointers remain[s] constant for a given input data rate and a feedback filtered distance between the write and read pointers." These pointers constitute the offsets between a first (write) clock and a second (read) clock.

Therefore, to maintain the distance between these pointers and synchronize the data clocked by the first clock to the second clock, the sample rate tracker resamples the data stream. Paragraph 8 of the provisional application goes on to disclose that the sample rate tracker is designed to "resample the input signal and then pick out the samples that are needed based on the error signal". Fractional resampling is specifically disclosed to "compute those samples needed for the outputs", Id. By way of example, one embodiment of the fractional resampling which may be performed by the rate tracker is disclosed wherein "if a desired output of 96.00001522587890625 kHz is needed for a given 96 kHz input, then one extra output is produced for every 65536 input samples", given that 00001522587890625^{-1} = 65536, Id.

Accordingly, the Applicants submit that the provisional application 60/136,685, filed on 5/28/99, discloses fractional resampling as detailed above and does so in a way that one of ordinary skill in the art could recognize that the Applicants invented what is claimed in the present Application. Consequently, the Applicants respectfully request that the filing date for the present Application be given at least the

filing date of the provisional application 60/136,685, namely 5/28/99.

The Examiner has rejected Claims 14-16 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, the Examiner alleges that Claim 14 fails to actually distinguish the generation of a first clock count and a second clock count. The examiner further alleges that the count as claimed could be looked [on] as a single count for both clocks.

The Applicants have amended Claim 14 to call in part for (underlining added for emphasis) ... "The method of claim of claim 1 wherein the offset derivation comprises counting at least a portion of a cycle of the first clock to produce a first clock count, counting at least a portion of a cycle of the second clock to produce a second clock count, generating an error signal as a function of the first clock count and the second clock count, the fractional resampling of the data being a function of the error signal."

As such, Amended Claim 14 now distinguishes the generation of a first clock count and a second clock count. Accordingly, Applicants submit that Claim 14 particularly points out and distinctly claim the subject matter which Applicants regard as the invention, and all rejections to Claim 14 have been overcome. Claims 15 and 16 are dependent on Claim 14, and are therefore also believed allowable based upon Claim 14.

The Examiner has rejected Claims 1-3, 6, 10, 17-19, 23, 27, 31, 37, 40, 42, 44, 48, 53, 57, 61 and 65 under 35 U.S.C. §102(e) as being anticipated by de Lantremange (U.S. Pat. No. 5,970,093) ("de Lantremange").

Applicants have amended Claim 1 to call for (underlining added for emphasis) ... "A method of synchronizing data clocked by a first clock to a second clock comprising deriving an offset between the first clock and the second clock, fractionally decimating the data during a data overflow and fractionally interpolating the data during a data underflow, wherein the data overflow and the data underflow are determined as a function of the offset."

De Lantremange does not show fractionally decimating or interpolating data during an underflow or condition, nor does it show that the data overflow and the data underflow are determined as a function of the offset in the manner claimed in the present Claim 1. Accordingly, the Applicants submit that Claim 1 is not anticipated by De Lantremange under 35 U.S.C. §102(e). Claims 2, 3, 6, 7 and 10-13 are dependent on Claim 1. As such, Claims 2, 3, 6, 7 and 10-13 are believed allowable based upon Claim 1 and for the additional limitations contained therein.

Applicants have amended Claim 17 to call for (underlining added for emphasis) ... "A method of synchronizing data exchanged between a cable modem and a cable head end comprising deriving an offset between a cable modem clock and a cable head end clock, fractionally decimating the data during a data

overflow and fractionally interpolating the data during a data underflow, wherein the data overflow and the data underflow are determined as a function of the offset."

De Lantremange does not show fractionally decimating or interpolating data during an underflow or condition, nor does it show that the data overflow and the data underflow are determined as a function of the offset in the manner claimed in the present Claim 17. Accordingly, the Applicants submit that Claim 17 is not anticipated by De Lantremange under 35 U.S.C. §102(e). Claims 18, 19, 21, 23 and 27-36 are dependent on Claim 17. As such, Claims 18, 19, 21, 23 and 27-36 are believed allowable based upon Claim 17 and for the additional limitations contained therein.

Applicants have amended Claim 37 to call for (underlining added for emphasis) ... "A synchronization circuit comprising a timing recovery clock adapted to be synchronized by an external source, a counter to count at least a portion of a cycle of the timing recovery clock, and a sample tracker adapted to receive sampled data, the sample tracker fractionally decimating the sampled data during a data overflow, and fractionally interpolating the data during a data underflow, wherein the data overflow and the data underflow are determined as a function of the count."

De Lantremange does not show fractionally decimating or interpolating data during an underflow or condition, nor does it show that the data overflow and the data underflow are determined as a function of the count in the manner claimed in

the present Claim 37. Accordingly, the Applicants submit that Claim 37 is not anticipated by De Lantremange under 35 U.S.C. §102(e). Claims 40 an 41 are dependent on Claim 37. As such, Claims 40 an 41 are believed allowable based upon Claim 37 and for the additional limitations contained therein.

Applicants have amended Claim 42 to call for (underlining added for emphasis) ... "A synchronization circuit comprising a sample tracker to receive a plurality of frames of sampled data from an external source, and a counter to count the frames of the sampled data, wherein the sample tracker fractionally decimates the sampled data during a data overflow, and fractionally interpolates the data during a data underflow, wherein the data overflow and the data underflow are determined as a function of the count."

De Lantremange does not show fractionally decimating or interpolating data during an underflow or condition, nor does it show that the data overflow and the data underflow are determined as a function of the count in the manner claimed in the present Claim 42. Accordingly, the Applicants submit that Claim 42 is not anticipated by De Lantremange under 35 U.S.C. §102(e). Claims 44-47 are dependent on Claim 42. As such, Claims 44-47 are believed allowable based upon Claim 42 and for the additional limitations contained therein.

Applicants have amended Claim 48 to call for (underlining added for emphasis) ... "A synchronization circuit, comprising a first counter to count at least a portion of a cycle of a first

clock, a second counter to count at least a portion of a cycle of a second clock, and a sample tracker adapted to receive sampled data, the sample tracker fractionally decimating the sampled data during a data overflow, and fractionally interpolating the data during a data underflow, wherein the data overflow and the data underflow are determined as a function of the error signal."

De Lantremange does not show fractionally decimating or interpolating data during an underflow or condition, nor does it show that the data overflow and the data underflow are determined as a function of the error signal in the manner claimed in the present Claim 48. Accordingly, the Applicants submit that Claim 48 is not anticipated by De Lantremange under 35 U.S.C. §102(e). Claims 51 and 52 are dependent on Claim 48. As such, Claims 51 and 52 are believed allowable based upon Claim 48 and for the additional limitations contained therein.

Applicants have amended Claim 53 to call for (underlining added for emphasis) ... "A synchronization circuit comprising error means for generating an error signal as a function of an offset between a first clock and a second clock and decimating means, adapted to receive sampled data, for fractionally decimating the sampled data during a data overflow, and interpolating means, adapted to receive sampled data, for fractionally interpolating the sampled data during a data underflow, wherein the data overflow and the data underflow are determined as a function of the error signal."

De Lantremange does not show fractionally decimating or interpolating means for fractionally decimating or interpolating during an underflow or condition, nor does it show that the data overflow and the data underflow are determined as a function of the error signal in the manner claimed in the present Claim 53. Accordingly, the Applicants submit that Claim 53 is not anticipated by De Lantremange under 35 U.S.C. §102(e). Claims 54, 57-67 are dependent on Claim 53. As such, Claims 54, 57-67 are believed allowable based upon Claim 53 and for the additional limitations contained therein.

Accordingly, in view of the above amendment and remarks it is submitted that the claims are patentably distinct over the prior art and that all the rejections to the claims have been overcome. Reconsideration and reexamination of the above Application is requested.

Respectfully submitted,
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